In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of providing emulation information indicative of internal operations of a data processor for use by an apparatus external to the data processor, comprising:

providing a stream of emulation trace information indicative of data processing operations performed by the data processor;

providing a stream of timing information indicative of operation of a clock used by the data processor to perform data processing operations, said timing information including cycle bits each indicating whether the data processor performed data processing operations or stalled during a corresponding clock cycle; and

inserting in the trace stream and in the timing stream temporal information indicative of a temporal relationship between the trace information and the timing information.

2. (Canceled)

3. (Currently Amended) The method of Claim ~~2~~ 1, wherein said inserting step includes inserting mutually corresponding identifiers in both the trace stream and the timing stream, and inserting in one of the streams an index for identifying a bit of the timing stream which represents a clock cycle that timewise corresponds to data in the trace stream at a point in the trace stream at which the trace stream identifier is inserted.

4. (Original) The method of Claim 3, wherein said index inserting step includes inserting said index into the trace stream.

5. (Original) The method of Claim 4, wherein said trace information includes program counter values associated with said data processing operations.

6 to 15. (Canceled)

16. (Original) The method of Claim 1, wherein said trace information includes memory reference information indicative of a memory access associated with said data processing operations.

17. (Canceled)

18. (Currently Amended) The method of Claim 1, ~~including~~ further comprising:

combining the trace stream and the timing stream into a single composite stream.

19. (Currently Amended) An apparatus for providing emulation information indicative of internal operations of a data processor for use by an apparatus external to the data processor, comprising:

a first input for coupling to the data processor;

a trace generator coupled to said first input for providing a stream of emulation trace information indicative of data processing operations performed by the data processor, said trace generator having a trigger input for receiving a trigger signal;

a second input for coupling to the data processor;

a timing generator coupled to said second input for providing a stream of timing information indicative of operation of a clock used by the data processor to perform data processing operations, said timing information including cycle bits each indicating whether the data processor performed data processing operations or

stalled during a corresponding clock cycle, said timing generator having a trigger input for receiving said trigger signal;

a table of sync ID numbers;

said trace generator operable when trigged by said trigger signal to insert temporal information corresponding to a next sync ID number from said table into the trace stream; and

~~said trace generator and~~ said timing generator ~~cooperable for inserting into the trace stream and~~ operable when trigged by said trigger signal to insert temporal information corresponding to said next sync ID number from said table into the timing stream ~~information indicative of a temporal relationship between the trace information and the timing information~~.

20. (Canceled)

21. (Currently Amended) The apparatus of Claim ~~20~~ 19, wherein said trace generator and said timing generator are cooperable for inserting mutually corresponding identifiers into the trace stream and the timing stream, respectively, one of said trace and timing generators further operable for inserting in its associated stream an index for identifying a bit of the timing stream which represents a clock cycle that timewise corresponds to data in the trace stream at a point in the trace stream at which the trace stream identifier is inserted.

22 to 24. (Canceled)

25. (Currently Amended) The apparatus of Claim 19, ~~including~~ further comprising:

a combiner coupled to said trace generator and said timing generator for combining said trace stream and said timing stream into a composite stream.

26. (Currently Amended) An integrated circuit, comprising:

a data processor for performing data processing operations;

an apparatus coupled to said data processor for providing emulation information indicative of said data processing operations to an emulation apparatus located externally of said integrated circuit, including a trace generator for providing a stream of emulation trace information indicative of said data processing operations, ~~and~~ a timing generator for providing a stream of timing information indicative of operation of a clock used by said data processor to perform said data processing operations, said timing information including cycle bits each indicating whether the data processor performed data processing operations or stalled during a corresponding clock cycle and a table of sync ID numbers; and

said trace generator operable to insert temporal information corresponding to a next sync ID number from said table into the trace stream; and

~~said trace generator and~~ said timing generator ~~cooperable for inserting into the trace stream and~~ operable to insert temporal information corresponding to said next sync ID number from said table into the timing stream ~~information indicative of a temporal relationship between the trace information and the timing information~~.

27. (Currently Amended) A data processing system, comprising:

an integrated circuit including a data processor for performing data processing operations;

an emulation controller located externally of said integrated circuit and coupled thereto for controlling emulation operations of said data processor;

said integrated circuit including an apparatus coupled between said data processor and said emulation controller for providing to

said emulation controller emulation information indicative of said data processing operations, said apparatus including a trace generator for providing a stream of emulation trace information indicative of said data processing operations, ~~and~~ a timing generator for providing a stream of timing information indicative of operation of a clock used by said data processor to perform said data processing operations, said timing information including cycle bits each indicating whether the data processor performed data processing operations or stalled during a corresponding clock cycle and a table of sync ID numbers; and

said trace generator operable to insert temporal information corresponding to a next sync ID number from said table into the trace stream; and

~~said trace generator and~~ said timing generator ~~cooperable for inserting into the trace stream and~~ operable to insert temporal information corresponding to said next sync ID number from said table into the timing stream ~~information indicative of a temporal relationship between the trace information and the timing information~~.

28. (Original) The system of Claim 27, including a man/machine interface coupled to said emulation controller for permitting a user to communicate with said emulation controller.

29. (Original) The system of Claim 28, wherein said man/machine interface includes one of a visual interface and a tactile interface.

30. (New) The method of claim 1, wherein:

said step of providing a stream of trace information includes formatting trace information into a plurality of packets having a fixed length;

said step of providing a stream of timing information includes formatting timing information into a plurality of packets having said fixed length; and

said inserting step includes formatting temporal information into a packet of said fixed length.

31. (New) The apparatus of claim 19, wherein:

said trace generator provides said trace information in packets having a fixed length and inserts temporal information in packets of said fixed length; and

said timing generator provides said timing information in packets having said fixed length and inserts temporal information in packets of said fixed length.

32. (New) The integrated circuit of claim 26, wherein:

said trace generator provides said trace information in packets having a fixed length and inserts temporal information in packets of said fixed length; and

said timing generator provides said timing information in packets having said fixed length and inserts temporal information in packets of said fixed length.

33. (New) The data processing system of claim 27, wherein:

said trace generator provides said trace information in packets having a fixed length and inserts temporal information in packets of said fixed length; and

said timing generator provides said timing information intpackets having said fixed length and inserts temporal information in packets of said fixed length.